DPDK
DATA PLANE DEVELOPMENT KIT

Flow and HQoS Acceleration Over DPDK Using Intel Programmable Acceleration Card N3000

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INTEL

Agenda

- Key Hardware Features

- DPDK and OPAE

- A Typical Flow and HQoS Acceleration Reference Design

- HQoS Acceleration
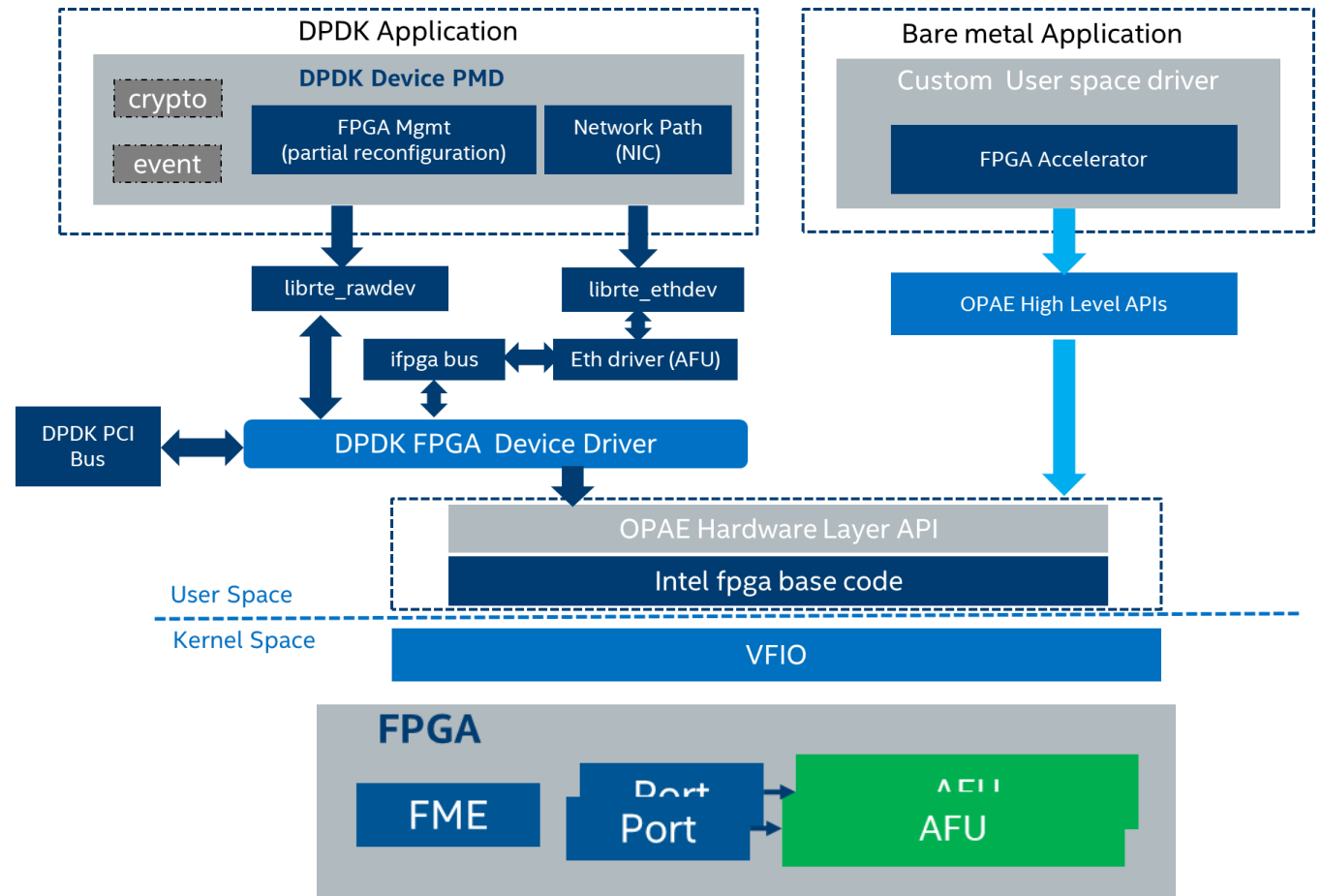
- Flow and HQoS Acceleration in DPDK

- Future work

Key Hardware Features

- ► Intel® Arria® 10 GT1150
  - 8x10GbE , 4x25GbE Network Interfaces
  - Local DDR4 and QDR Memory
- ► Dual Intel® Ethernet Controller XL710
  - Extensive OS support and Easier system integration
  - XL710 enable and XL710 bypass
- ► PCIe Interface
  - 2 x PCIe Gen3x8 host interface
  - 2xPCIe Gen3x8 towards the FPGA
  - PCIe Gen3x8 towards each of the XL710
  - PCIe SMBus connected MAX10 and all XL710
- ► Intel® MAX® 10 CPLD
  - Board power, clocks and reset control
 - Board security and management
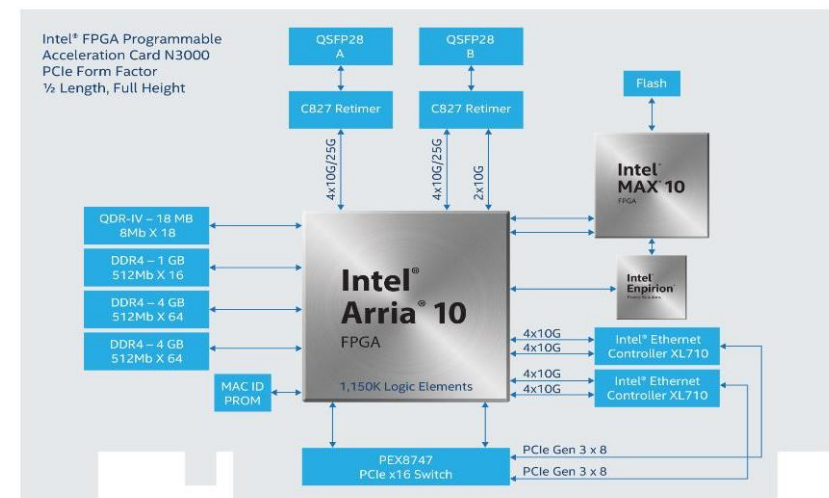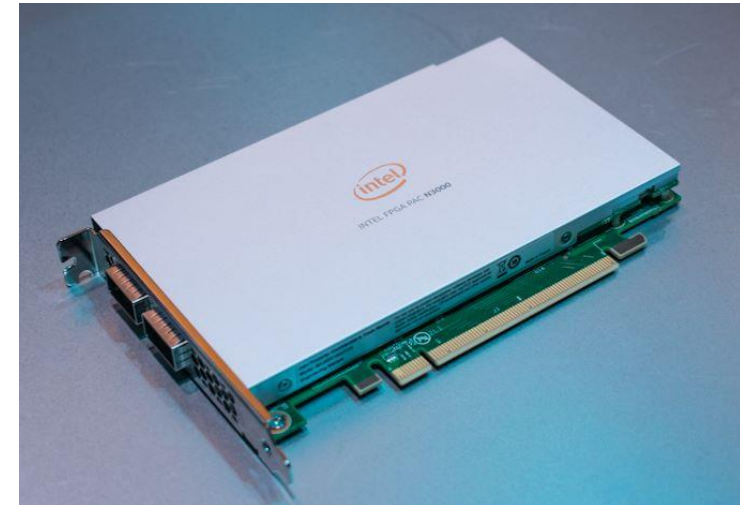
DPDK and OPAE

- ► AFU devices are handled by PMDs
  - ▪ AFUs provide acceleration functions
  - ▪ AFUs are scanned and probed on the IFPGA bus
- ► RawDev is a special kind of Drivers to manage FPGA device
  - ▪ AFU PCIe MMIO address map
  - ▪ OPAE UMD(User Mode Driver) integration
- ► FPGA management ops are handled by OPAE user space driver
  - ▪ Enumerate/identify AFUs on the IFPGA bus
  - ▪ FPGA thermal/power management
  - ▪ FPGA performance reporting
  - ▪ AFU PR (when HW support is available)

A Typical Flow and HQoS Acc. Reference Design
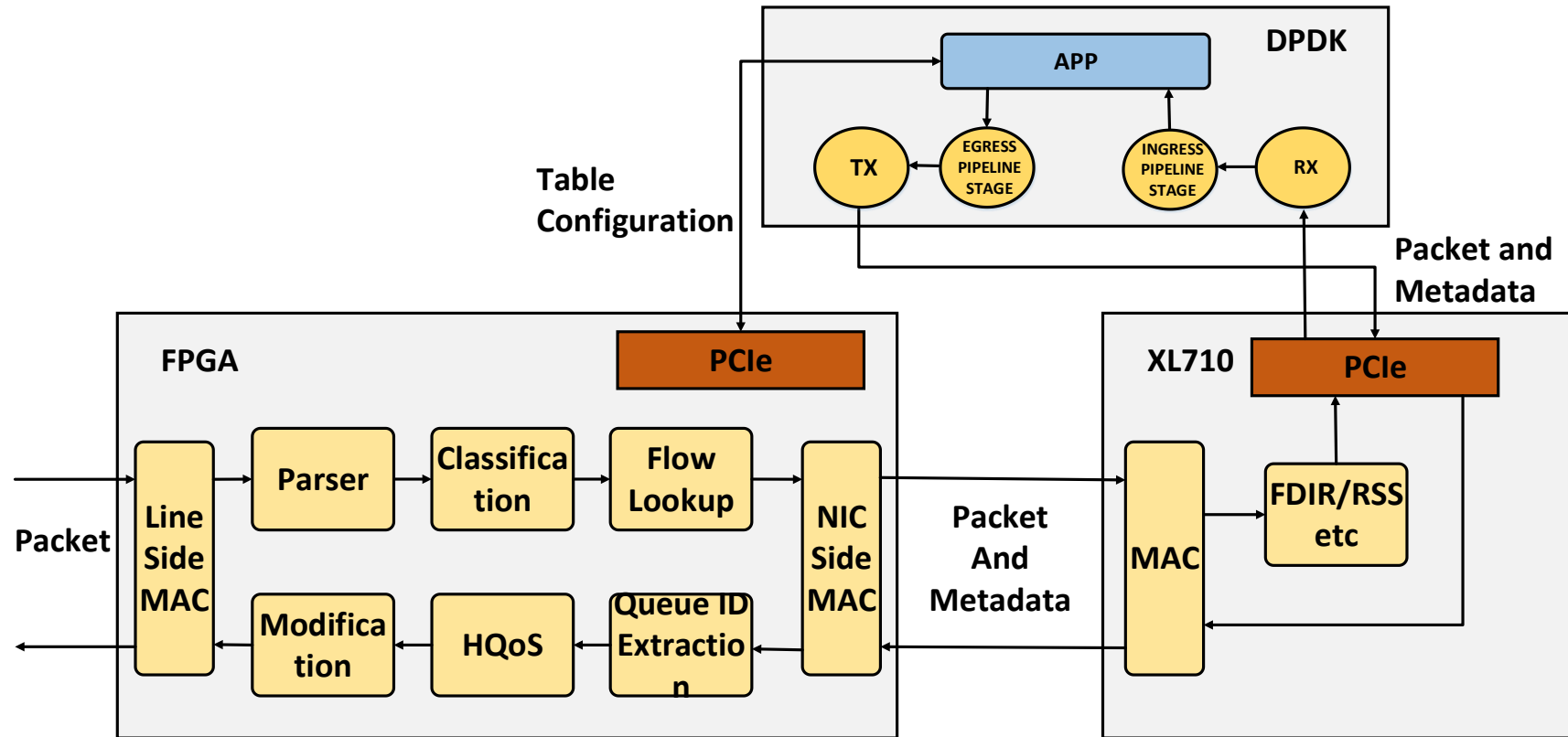
- ▶ Ingress Flow Partial Offload
  - ▪ Flow search data in metadata
  - ▪ DPDK parse metadata

- ▶ Egress Flow Based HQoS
  - ▪ Flow is identified by Queue ID
- ▶ DPDK Pipeline Handle other Packet Processing

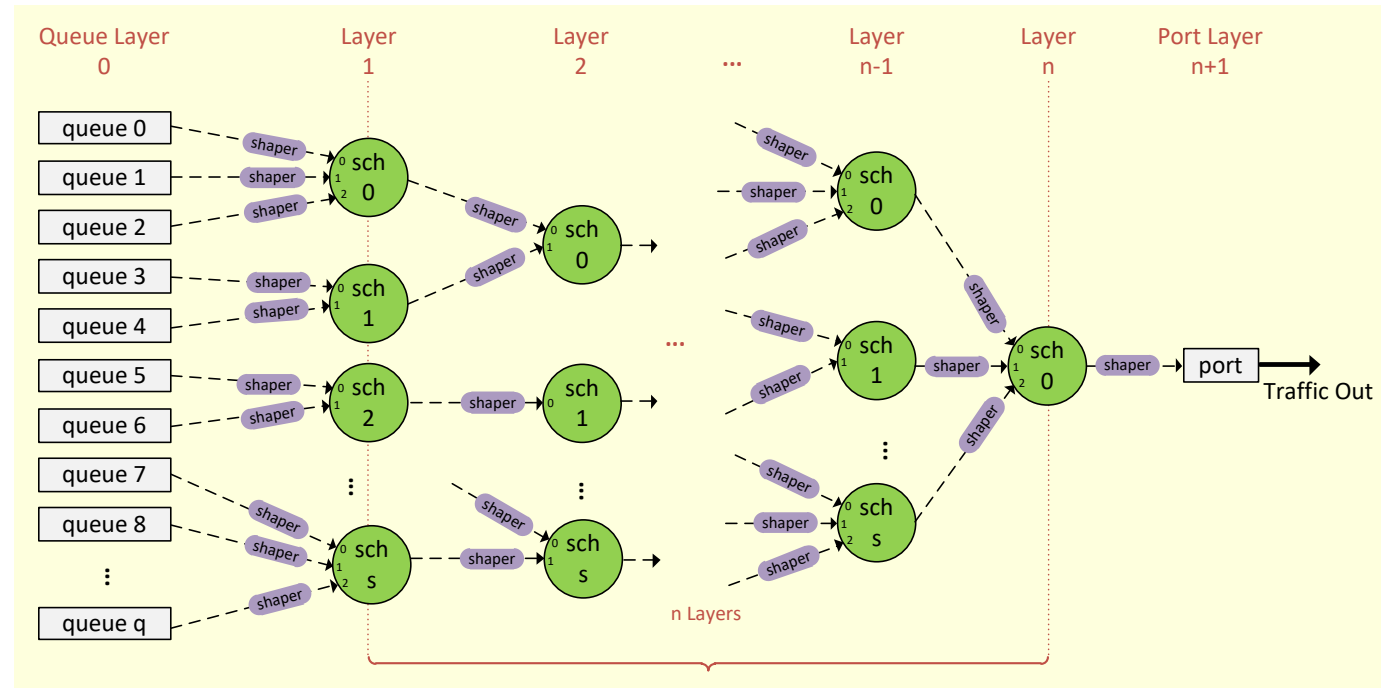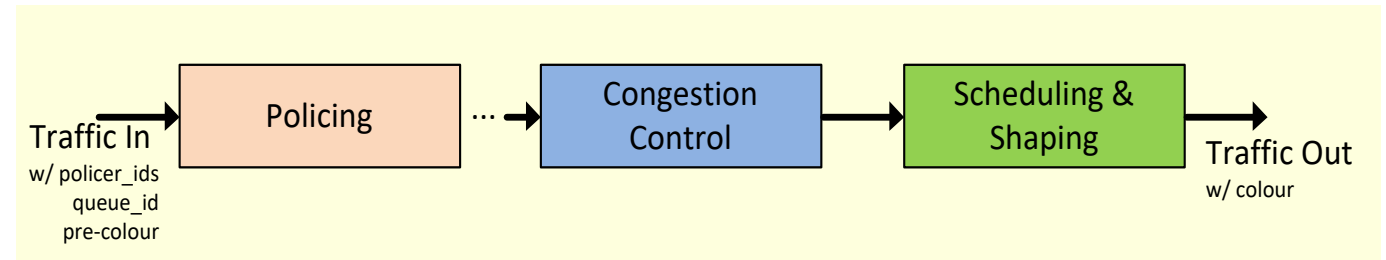# HQoS Acceleration

- ► Capacity
  - Policing
  - Congestion Control
  - Scheduling and Shaping
- ► Queuing
  - Flow match for Queue ID
 - Queue ID in Metadata
  - Thousands of Queue Number
- ► Configuration
  - Follow Rte_tm API
  - Testpmd and Example APP

Flow and HQoS Acc. in DPDK

- ▶ I40e PMD handles Packet TX/RX in XL710 enable mode
  - New PF Device ID
  - Reuse current code
  - Binding I40e PF to FPGA Port
- ▶ AFU PMDs provide data plane control path
  - Binding FPGA Port to I40e PF
  - Implement HQoS and Flow Acceleration
  - Follow librte_ethdev API
- ▶ DPDK Test APP
  - Simple Test APP for HQoS, Flow and Packet TX/RX
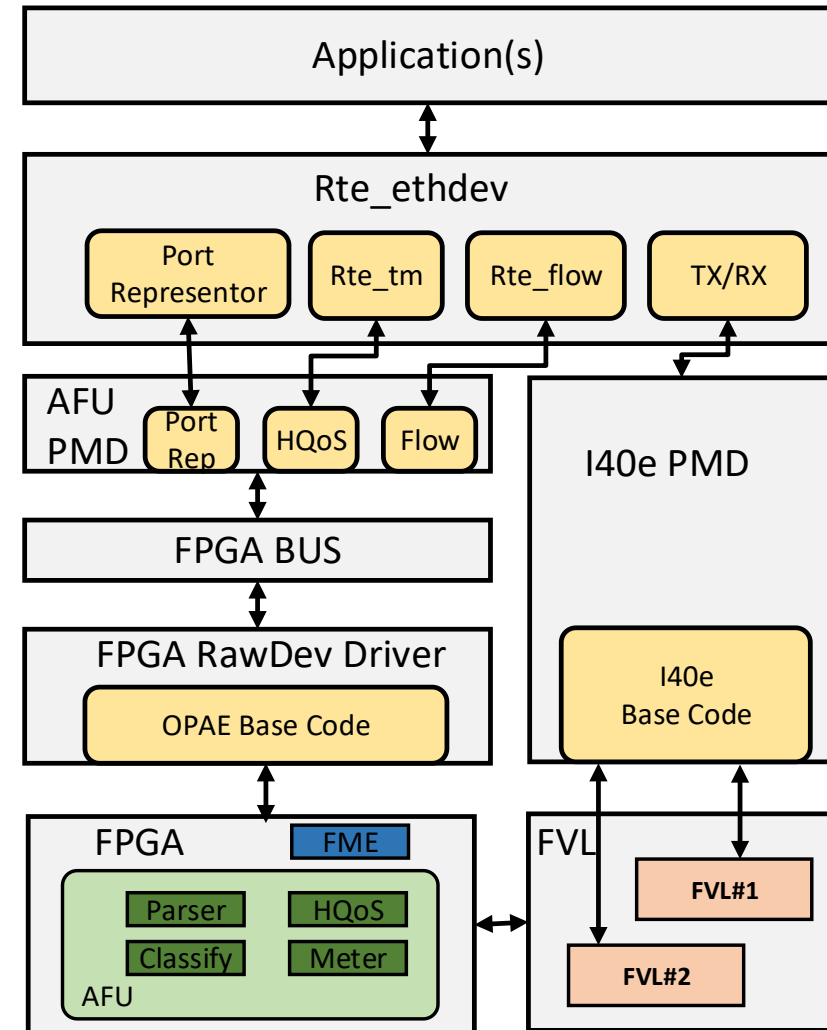
Future work

- ► Enable more workload
  - ▪ vBNG/vBRAS
  - ▪ 5G FlexRan
  - ▪ vRouter
- ► PAC N3000 Power Management

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Thanks